USN | | | | | | | | | | | **10CS72**

Seventh Semester B.E. Degree Examination, June/July 2023
Embedded Computing Systems

Time: 3 hrs.   Max. Marks:100

Note: *Answer any FIVE full questions, selecting at least TWO questions from each part.*

PART – A

1 a. List and explain the challenges of embedded computing system design.   (07 Marks)
   b. Explain the sequence diagram for transmitting a control input in model train controller.
                                                                                      (07 Marks)
   c. Write GPS moving map requirement chart.   (06 Marks)

2 a. What is cache? How it relates to memory system mechanism? Explain different types of cache miss.   (08 Marks)
   b. Solve the following:
      (i) What is the average memory access time of machine whose hit rate is 93% with cache access time of 5 ns and main memory access time of 80 ns?
      (ii) Calculate cache hit rate, if the cache access time is 5 ns, average memory access time is 6.5 ns and main memory access time is 80 ns.   (05 Marks)
   c. What is interrupt? Explain with neat diagram interrupt mechanism.   (07 Marks)

3 a. What is bus? Write the major components of bus protocol. Explain burst read transaction with neat diagram.   (10 Marks)
   b. Explain with neat diagram the bus with DMA controller.   (06 Marks)
   c. Write ARM assembly code for below C statement $z = (x \mid 22)$ and $(y >> 2)$ (04 Marks)

4 a. Sketch and explain dataflow and control data flow (CDFG) graph for programming model.
                                                                                      (10 Marks)
   b. Sketch CDFG for following C code statement:
      if (a + b > 0)
          X = S;
      else
          X = 7;   (04 Marks)
   c. Explain briefly types of performance measures on programs.   (06 Marks)

PART – B

5 a. Define process. With neat diagram, explain memory organization and state transition of process.   (10 Marks)
   b. What is multitasking? Explain the types of multitasking.   (04 Marks)
   c. Distinguish between process and thread.   (06 Marks)

6 a. Define IPC. Explain the IPC mechanism adopted by different operating systems.   (10 Marks)
   b. Explain system architecture of telephone answering machine.   (05 Marks)
   c. Write digital telephone answering machine requirement form.   (05 Marks)

7 a. Explain hardware and software architecture of distributed system.   (05 Marks)
   b. Explain multihop communication with a neat diagram.   (05 Marks)
   c. Explain IP Packet Structure and Internet Service Stack with neat diagram.   (10 Marks)

8 a. Explain various hardware debugging tools used in embedded product development.
                                                                                      (08 Marks)
   b. Explain monitor program based firmware Debugging and Incircuit Emulator (ICE) based firmware debugging.   (12 Marks)

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